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TRANSISTOR SINE-WAVE *LC* OSCILLATORS

Some General Considerations and New Developments

By P. J. BAXANDALL, B.Sc.(Eng.).

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SUMMARY

The paper begins by showing that various well-known simple oscillator circuits, usually analysed separately, are essentially equivalent to one another if certain reasonable assumptions are made, and appreciation of this fact simplifies the design problem.

A discussion follows concerning class-C oscillators and the difficulty of combining high efficiency with a satisfactory degree of independence of transistor parameters. The problem of avoiding squegging is also considered.

A simple push-pull high-efficiency oscillator is then described, in which substantially constant current flows in each transistor for the whole of its 180° conduction angle. This oscillator is believed to possess a unique combination of desirable features.

Another unusual high-efficiency oscillator is then presented, which is more elaborate than the previous one but which has advantages in certain respects.

The paper ends with a description of an oscillator based on the 'long-tailed-pair' circuit. The oscillator is exceptionally easy to design and make, and is suitable for applications where high efficiency is not important. It can supply either a sine wave or a square wave, or both.

(1) THE EQUIVALENCE OF VARIOUS WELL-KNOWN OSCILLATOR-CIRCUIT CONFIGURATIONS

Fig. 1 shows several simple transistor oscillator circuits, in which irrelevant details have been omitted.

That these circuits are really all equivalent to one another, assuming the coils to be tightly coupled magnetically,* may be seen by appropriately redrawing some of them. Since the h.t. supply leads are at the same a.c. potential, they may be joined together in a circuit diagram concerned only with a.c. conditions. Thus Fig. 1(*a*) may be drawn as in Fig. 2(*a*), when the two windings are seen to constitute effectively an auto-transformer with the tuning capacitor and load across the top section. A redrawn version of Fig. 1(*b*) is the same except that the load and tuning capacitor are connected across the lower part of the auto-transformer. On redrawing Fig. 1(*c*), Fig. 2(*b*) is obtained, and here the arrangement of windings shown (same direction of turns from terminal 1 through to terminal 4) is equivalent to connecting the emitter to a tapping between 1 and 2, as shown dotted. With this modification the circuit is equivalent to Fig. 2(*a*) but with the tuning capacitor and load across the total auto-transformer winding; equivalent capacitor and load values may, of course, be determined for connection across only one section of the auto-transformer. It may further be observed that Fig. 2(*b*), with dotted modification, is the same as the Hartley circuit of Fig. 1(*e*) except for the position of the earth connection, the latter being of no consequence for analytical purposes.

Redrawing Fig. 1(*d*) gives Fig. 2(*c*), and the coil between 1 and 2 in the latter may be removed and replaced by an equivalent tapping on the coil between 3 and 4 as shown dotted. The circuit is then seen to be equivalent to the others except for the position of the earth connection.

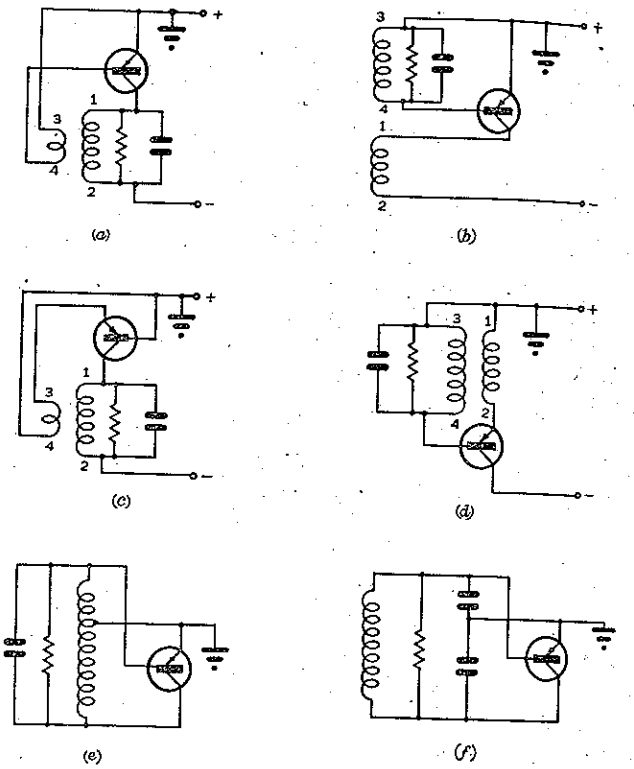

Fig. 1.—Some simple oscillator circuits.

With regard to Fig. 1(*f*), the question is really to what extent a capacitive tapping on a tuned circuit is equivalent to a tapping on the coil, and the exact equivalence of the two circuits shown in Fig. 3 is thought to provide the simplest basis for the comparison.* So long as the reactance of $(C_a + C_b)$ in Fig. 3(*b*) is small enough for the voltage across it to be negligible in comparison with other voltages in the oscillator circuit, there will be no significant difference in behaviour between circuits such as Figs. 1(*e*) and (*f*), provided that the tapping ratio and total inductance are the same in each. For a given load resistance R_L, the higher the loaded Q-factor is made the smaller must be L and the larger $(C_a + C_b)$. It is evident that, with a sufficiently large loaded Q-factor, the reactance of $(C_a + C_b)$ can be made very low indeed compared with the dynamic resistance of the tuned circuit referred to the terminals B and D. In most circumstances, except when the loaded Q-factor is very low, for example 10, it will be found that the presence of the effective capacitance $(C_a + C_b)$ in series with the emitter lead has a fairly negligible

* This assumption is usually justified nowadays, because air-cored coils are much less widely used than in the past.

Mr. Baxandall is at the Royal Radar Establishment.

* The method may be extended to circuits of the Gouriet or Clapp type,[1,2] having three series capacitors across the coil.

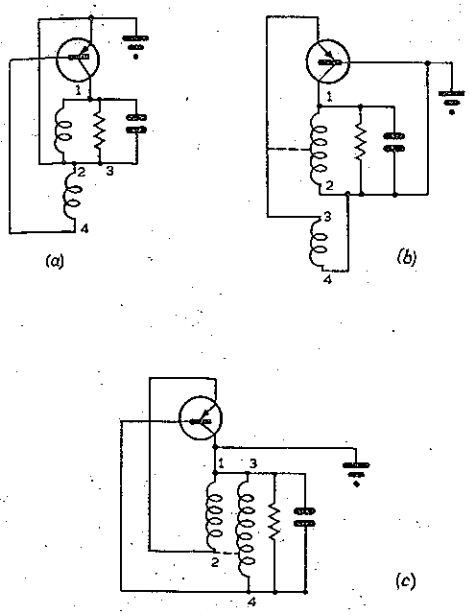

Fig. 2.—Redrawn oscillator circuits.

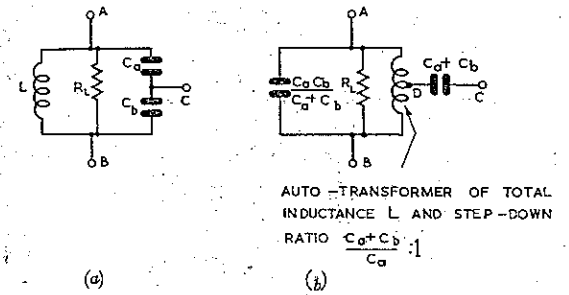

Fig. 3.—Equivalent circuits for 'capacitance tap'.

influence; it merely introduces a slight phase shift which is compensated by a slight shift of the operating frequency.

Thus, to summarize, any of the ordinary simple transistor oscillator circuits may be regarded as consisting essentially of a 3-terminal transistor* connected to the three terminals of a tuned auto-transformer, the tuning capacitor and load being connected to any pair of terminals on this auto-transformer, or a second winding coupled to it, and any convenient point being earthed.

The terms 'common emitter', 'common base' and 'common collector' have little significance, since the input and output circuits are not separate in these simple oscillators, but constitute one circuit owing to the (ideally) 100% magnetic coupling. However, the terms 'earthed' emitter, base and collector, respectively, which in amplifier circuits usually have the same significance as the above, are applicable to oscillators, but are concerned only with the practical question of the choice of earthing point.

The realization that a number of apparently different circuit configurations are, in fact, equivalent is valuable for two reasons:

(*a*) The designer is free to choose his circuit configuration on the basis of various practical considerations, without the complication of feeling that the choice necessarily affects the theoretical performance.

(*b*) It is immediately evident that a circuit such as Fig. 1(*d*), which might be described as an emitter-follower oscillator, has no theoretical advantages due to (apparently) employing the transistor as an emitter follower. That confusion of thought has been caused by matters such as this may be seen from Reference 3.

* In a practical circuit, where the bias components may sometimes have an appreciable a.c. impedance, the latter may be allowed for by incorporating it into the equivalent circuit of the transistor.

(2) CLASS-C OSCILLATORS

(2.1) General

In this Section some basic features of conventional transistor class-C oscillators are discussed. Whilst it is hoped that the discussion may be useful in itself, the primary aim is to point out the shortcomings of these oscillators and thus set the scene for introducing some improved circuits in later Sections.

(2.2) Base-Current-Biased Circuits

A transistor, in striking contrast to a valve, passes substantially no current at zero bias voltage, so that means must be provided to bias it on initially if self-starting of oscillation is to be obtained when the h.t. supply is switched on. For efficient class-C operation, however, a large bias in the opposite direction is necessary. This may be produced by rectification, in a manner comparable with the usual arrangement in a valve oscillator, by including a resistor and capacitor in the base circuit. The simplest arrangement which satisfies both these requirements is shown in Fig. 4(*a*), and is capable of overall power-conversion efficiencies well above 70%. The turns ratio is typically 2. R_b should normally be adjusted to give appreciable bottoming,* since this very effectively stabilizes the output-voltage amplitude; in many cases it is reasonable to reduce R_b to about half the value at which bottoming commences. Excessive bottoming should be avoided, however, since it gives reduced efficiency, increased dissipation of power in the transistor and increased distortion.

The circuit of Fig. 4(*a*), in common with others in which the bias is produced by the flow of base current, has the undesirable feature that the degree of bottoming is greatly affected by the value of the common-emitter current-gain factor, α', for the particular transistor used. In practice, it is necessary to adjust R_b to suit the transistor sample.

A further undesirable feature of the circuit of Fig. 4(*a*),

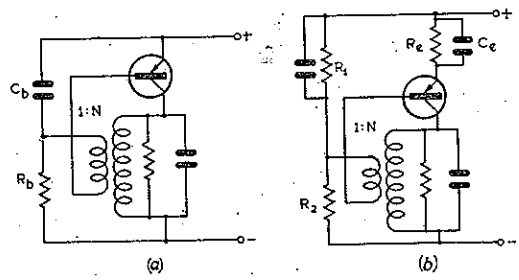

Fig. 4.—Class-C oscillator circuits.

especially in very low-power versions, is that the degree of bottoming is considerably affected by variations in the base-collector leakage current, I_{c0}. An increase in I_{c0} is equivalent to raising the current in R_b, and results in an increase in the amplitude of the base-current pulses and hence in the degree of bottoming, i.e. the bottoming dip in the collector-current waveform becomes larger. Thus the circuit is not well suited to situations where wide variations in ambient temperature are

* A transistor is said to be bottomed when the collector-emitter voltage is so low that the operating point is below the knee of the collector-current/collector-voltage characteristic; the collector current is then almost unaffected by small changes in base current. When bottoming occurs in a class-C oscillator, a dip appears in the top of the collector-current-pulse waveform, owing to there being insufficient collector voltage, for a fraction of the duration of the pulse, to maintain the full current. With excessive bottoming, this dip becomes so large that reverse collector current flows during the central part of the pulse.

expected, and variations in α' and I_{c0} during the life of the transistor should also be considered. Nevertheless the circuit has the virtues of simplicity and cheapness combined with high efficiency, and provided that it is run with a fairly high degree of bottoming, the disadvantages just mentioned are not always serious.

(2.3) Emitter-Current-Biased Circuits

A circuit which is usually much preferable to that of Fig. 4(*a*) is shown in Fig. 4(*b*). Depending on the component values used, the circuit may or may not operate under class-C conditions, but these conditions are assumed here. In the circuit of Fig. 4(*b*), the bias required for class-C operation is produced by the emitter current flowing in R_e, R_1 and R_2 preferably providing only the small amount of negative bias that is necessary to ensure reliable self-starting. This is typically 0·3 volt with a normal germanium transistor. The impedance of the base-bias network should preferably be low enough to ensure that only insignificant voltage changes occur across this network when base current flows during oscillation.

The effects of changes in α' and I_{c0} are very much less in this circuit than in the previous one, since the base current now adjusts itself automatically until the emitter current is sufficient to give a voltage across R_e nearly equal to the peak negative value of the voltage waveform applied to the base.

The main disadvantage of the circuit, compared with that of Fig. 4(*a*), is that a substantial fraction of the h.t. power supplied is dissipated in R_e, giving reduced overall efficiency. If the collector dissipation is to be kept to a minimum for a given power output, the turns ratio, N, should be made small, so that a small angle of flow is obtained, but this reduction in transistor dissipation is achieved at the expense of an increased power loss in R_e. There is thus a value of N that gives maximum overall efficiency in any given situation. With $N = 2$, an overall efficiency of 60% can be achieved in practice.

(2.4) Avoidance of Squegging

A further factor which complicates the design of these circuits is the necessity to avoid squegging. The squegging mechanism is discussed in some detail in Reference 4, and space permits only a brief statement of some facts. In the circuit of Fig. 4(*b*), if, after establishing normal oscillating conditions, the emitter current were suddenly to stop flowing, the bias voltage would fall exponentially towards approximately zero, with a time-constant R_eC_e, and the tuned-circuit oscillatory voltage amplitude would fall with a decrement time-constant, τ_d, given by

$$\tau_d = \frac{Q}{\pi f_0} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (1)$$

where Q = Loaded Q-factor of the tuned circuit.
f_0 = Frequency of oscillation.

If R_e is adjusted to give an amplitude of oscillation insufficient to cause bottoming, it is approximately true that squegging will not occur if R_eC_e is less than τ_d. A detailed analysis of the problem yields a result more complicated than this, but the above criterion is a useful practical guide, and no transistor oscillator on which the author has experimented has failed to squegg if R_eC_e has been made equal to $2\tau_d$, nor has it failed to give continuous oscillation if R_eC_e has been made equal to $\frac{1}{2}\tau_d$.

The same result may be applied to class-C oscillators in which the bias is produced by a base resistor and capacitor, provided that the resistor is returned approximately to emitter potential. However, in the circuit of Fig. 4(*a*) the bias resistor R_b is not returned to emitter potential, but to the h.t. negative supply, and the above rule is then not directly applicable. The fundamental factors involved in determining whether or not squegging will occur are not the time-constants as such, but the initial rates at which the bias voltage and the amplitude of the oscillatory voltage fed back to the base decay if transistor current ceases. If the cessation of current were to occur at $t = 0$, the equation for the subsequent variation in the amplitude, $\hat{v}$, of the voltage fed back to the base circuit is

$$\hat{v} = \frac{\hat{V}}{N}\varepsilon^{-t/\tau_d} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (2)$$

where $\hat{V}$ is the initial peak amplitude at the collector. The initial rate of change of $\hat{v}$ is obtained by differentiating eqn. (2) and is

$$\left[\frac{d\hat{v}}{dt}\right]_{t=0} = -\frac{\hat{V}}{N\tau_d} \quad . \quad . \quad . \quad . \quad . \quad . \quad (3)$$

The initial rate of change of bias voltage, v_{bias}, is given by

$$\left[\frac{dv_{bias}}{dt}\right]_{t=0} = -\frac{I_{bias}}{C_b} \quad . \quad . \quad . \quad . \quad . \quad . \quad (4)$$

where I_{bias} is the current initially flowing in R_b in Fig. 4(*a*), and is given approximately by

$$I_{bias} = \frac{V_{ht} + \frac{\hat{V}}{N}}{R_b} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (5)$$

Substituting eqn. (5) in eqn. (4),

$$\left[\frac{dv_{bias}}{dt}\right]_{t=0} = -\frac{V_{ht} + \frac{\hat{V}}{N}}{R_bC_b} \quad . \quad . \quad . \quad . \quad (6)$$

From eqns. (3) and (6) the approximate criterion is that no squegging will occur provided that

$$\frac{V_{ht} + \frac{\hat{V}}{N}}{R_bC_b} > \frac{\hat{V}}{N_d} \quad . \quad . \quad . \quad . \quad . \quad . \quad (7)$$

$\hat{V}$ will normally be approximately equal to V_{ht}, i.e. the transistor will be nearly bottoming, so that eqn. (7) may then be simplified, giving the criterion that no squegging will occur provided that

$$R_bC_b < (1 + N)\tau_d \quad . \quad . \quad . \quad . \quad . \quad . \quad (8)$$

It is evident that the circuit of Fig. 4(*a*) is no more prone to squegging, with a given value of C_b, than a circuit with the same value of C_b but having a smaller value of R_b returned to approximately emitter potential, assuming the same base current in each case. This conclusion has been verified experimentally. The circuit of Fig. 4(*a*) has the advantage of using the minimum number of components. The only disadvantage is that the power dissipated in R_b is greater, but since this is often less than 5% of the output power, it is not usually a very important consideration.

In the above discussion of squegging it has been assumed that bottoming does not occur. If pronounced bottoming is present, however, it has a very potent stabilizing influence on the squegging mechanism, since any small reduction in output voltage which may occur immediately increases the collector current, owing to reduced bottoming, to a much greater extent than the reduction in base drive reduces the collector current. Thus, an oscillator which operates with pronounced bottoming can employ a much larger bias capacitance than is permissible

when there is little or no bottoming, but it is not normally recommended that this condition of operation be employed.* For all normal applications the bias capacitance should be not more than half the value indicated by the above squegging criterion. However, if the bias capacitance is unnecessarily small, the alternating voltage across it becomes so large that the angle of flow of base current is considerably increased, with a consequent reduction in efficiency. When the loaded Q-factor of the tuned circuit is low, which it must be to minimize tuned-circuit losses, the largest bias capacitance permitted by squegging considerations is smaller than one would otherwise like to use, and is one of the reasons why it is difficult to achieve angles of flow much less than about 70° when the loaded Q-factor is about 10.

(3) IMPROVED HIGH-EFFICIENCY OSCILLATORS: GENERAL APPROACH

For high-efficiency operation in any transistor oscillator, it is axiomatic that, when current flows through a transistor, the voltage across it should be as small as possible, in order to minimize the power dissipation in the transistor.

In the class-C oscillator, since the voltage across the transistor varies approximately sinusoidally, it is necessary to switch the transistor on only during the very short time intervals for which the transistor voltage is nearly zero. This inevitably leads to difficult design compromises, as described in Section 2.

In general, what is required for improved performance is to add some suitable non-power-dissipating elements between the transistor(s) and the tuned circuit, in order to allow the transistor voltage to remain small during the whole of a long conduction time and yet to permit the tuned circuit meanwhile to execute a sinusoidal oscillation.

One idea,[6] which occurred independently to the author as a result of reading Reference 5, involves the addition of one or more low-loss parallel-tuned circuits, tuned to harmonic frequencies, between the transistor(s) and the main tuned circuit. This scheme did not seem to offer as complete and simple a solution as those described in Sections 4 and 5, and, in view of the practical success of the latter when using transistors, it was abandoned.

In the push-pull oscillator of Section 4, the full transistor current is flowing at the time when conduction is being switched over from one transistor to the other, but there is very little voltage across either transistor; the oscillator has therefore been termed a *current-switching oscillator*.

In the push-pull oscillator of Section 5, very little transistor current is flowing at the time when conduction is being switched over from one transistor to the other, but large voltages exist across one or both transistors; the oscillator has therefore been termed a *voltage-switching* oscillator.

In both oscillators very little power dissipation occurs in the transistors during the switch-over time.

It is suggested that the term 'class-D' should be applied to the operating conditions used in these oscillators. Thus a class-D oscillator or amplifier is one in which the angle of current flow in each active device is 180°, but in which substantially no voltage exists across the active device while it is conducting.

(4) HIGH-EFFICIENCY CURRENT-SWITCHING OSCILLATOR†

(4.1) Advantages of the Circuit

The circuit arrangement of Fig. 5 is believed to be unique in possessing a number of desirable features not to be found in combination in any other circuit. These are as follows:

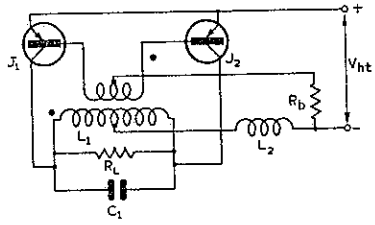

Fig. 5.—Basic circuit for current-switching oscillator.

(*a*) High overall efficiency, typically 80%.
(*b*) Compared with a class-C oscillator, more power output may be obtained from a given pair of transistors without exceeding the collector-dissipation rating.
(*c*) Large variations in transistor parameters and ambient temperature can be tolerated without significant effect on performance.
(*d*) The oscillator has very few components and is very easy to build.
(*e*) The design calculations are much simpler than for a class-C oscillator.
(*f*) The output voltage varies very little between full load and no load, and the feed current at no load is very small.
(*g*) The harmonic distortion for a given loaded Q-factor is considerably less than in a push-pull class-C oscillator; the even harmonics are very low indeed.
(*h*) There is only a small amount of ripple in the h.t. current, and so the by-pass capacitor, which is normally necessary in a class-C oscillator, may often be omitted.

(4.2) Principle of Operation

Each transistor conducts for the whole of a half period, i.e. the angle of flow is 180°, and while conducting the transistor is in a bottomed state, so that there is very little collector dissipation. The collector current is nearly constant during the conduction time, owing to the presence of the choke L_2, which would ideally be of infinite inductance. This almost constant current is switched from one transistor to the other by the voltage from the feedback winding, whose value is not critical.* The base current of each transistor is determined, to a first order, by the value of R_b and the h.t. voltage only, and is made sufficient to keep the transistor bottomed, with an adequate margin to spare, at a collector current corresponding to the desired full output power.

Assuming that the loaded Q-factor of the tuned circuit is high enough to give a reasonably close approximation to a sine-wave voltage across the tuned circuit (a Q-factor of 10 is usually suitable, giving a third-harmonic content of just over 1%), the waveform of the voltage between the collector-winding centre tap and the h.t. positive supply will be approximately as shown in Fig. 6. The mean value of this waveform is $(2/\pi)V_{max}$, and

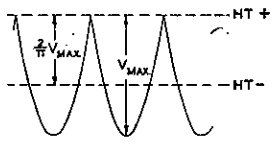

Fig. 6.—Waveform at centre-tap of collector winding in circuit of Fig. 5.

since no direct voltage can exist across the choke, which is assumed to be of zero resistance, the sine-wave amplitude must adjust itself so that the following relationship is satisfied:

$$\frac{2}{\pi}V_{max} = V_{ht} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (9)$$

* When operating in this condition a curious mode can occur in which only alternate collector-current pulses have a bottoming dip, and the output voltage then contains a small amount of sub-harmonic.

† The oscillators described in Sections 4 and 5 are the subject of British Patent Application No. 8865, 1959.

* A turns ratio of about 10 : 1 between the whole collector winding and the whole base winding is normally suitable. If this ratio is made too small, the power dissipated in R_b is considerably increased.

The peak sine-wave voltage between collectors is $2V_{max}$, so that the r.m.s. value is $\sqrt{2}V_{max}$. From eqn. (9) then follows the convenient design formula:

$$\text{R.M.S. voltage between collectors} = \frac{\pi}{\sqrt{2}}V_{ht}$$

$$= 2{\cdot}22V_{ht} \quad . \quad . \quad . \quad (10)$$

The actual voltage obtained will be a few per cent less than this, since the collector-emitter voltage drop when bottomed, and also the direct-voltage drop in L_2, have been neglected.

The peak collector-emitter voltage applied to each transistor when it is in the non-conducting state is given approximately by

$$(V_{ce})_{max} = \pi V_{ht} \quad . \quad . \quad . \quad . \quad . \quad . \quad (11)$$

and the h.t. voltage must be low enough to avoid exceeding the collector-voltage rating of the transistors.

Ideally (assuming all reactances to be lossless and the transistors to be ideal switches), the only place where unwanted power dissipation occurs is in R_b, but this power loss may be less than 5% of the output power. The power dissipated may, however, be considerably reduced, if desired, by inserting a choke in the feedback-winding centre-tap lead and connecting the choke to the h.t. positive supply through a series combination of a diode and a resistor of much smaller value than that of R_b in Fig. 5; the choke ensures constant base current and the resistance determines the value of this constant current. An additional resistor connected to the h.t. negative supply is also necessary, in order to provide negative bias to make the circuit self-starting, but this additional resistor will consume only a very small amount of power. The expense of this extra choke, diode and resistor, which give only a small increase in efficiency, will probably make the circuit arrangement of Fig. 5 usually the most suitable choice, except perhaps in oscillators with output powers in excess of a few watts.

(4.3) Harmonic Distortion

Since the tuned circuit is fed effectively with a current of square waveform, this current ideally contains no even harmonics, and the third harmonic has an amplitude one third of the fundamental. The third-harmonic distortion in the output voltage is given approximately by

$$\frac{100}{8Q}\% \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (12)$$

where Q = Loaded Q-factor of the tuned circuit.

(4.4) Choice of Choke Value

Whereas L_2 in Fig. 5 would ideally be infinite, the main effect of a finite inductance is merely to cause the current in each transistor to vary throughout the conduction time, and, provided that the transistor stays bottomed, there is no great loss of efficiency.

In Section 9.1 it is shown that the peak-to-peak amplitude of the current waveform in L_2 is given by

$$I_{pp} = 0{\cdot}421\frac{V_{max}}{\omega L_2} \quad . \quad . \quad . \quad . \quad . \quad . \quad (13)$$

where $\omega = 2\pi \times$ (oscillator frequency).

Using eqn. (9) this result may alternatively be expressed as

$$I_{pp} = 0{\cdot}661\frac{V_{ht}}{\omega L_2} \quad . \quad . \quad . \quad . \quad . \quad . \quad (14)$$

A satisfactory practical design rule is to make L_2 at least large enough to limit the peak-to-peak current fluctuation in it to about a quarter of the mean h.t. current, and Section 9.1 shows that this figure is achieved when the reactance of L_2 at the oscillator frequency is about half the collector-to-collector load resistance, R_L. If a loaded Q-factor of 10 is adopted, which is a suitable choice for most applications, L_2 should be at least five times the collector-to-collector tuned-circuit inductance* L_1. Under these conditions, Section 9.2 shows that the magnetic energy stored in L_2 is approximately 13% of the peak energy stored in L_1. It is not difficult to design L_2 so that the sum of its d.c. and a.c. losses is well under 5% of the oscillator output power without making L_2 physically larger than the tuned-circuit inductor.

(4.5) Effect of Hole Storage

An important point in the operation of this oscillator is that, whereas the mean base current is fairly closely determined by R_b and V_{ht}, it is possible, owing to hole-storage effects, for much larger instantaneous base currents to flow during the short time that current is being switched over from one transistor to the other. Thus when transistor J_1 is being switched off, a large reverse base current of transient nature may flow into its base from the base of J_2, thereby rapidly clearing the minority-carrier hole concentration in J_1 and injecting holes into J_2, which therefore bottoms quickly. This ability to supply large transient currents in the emitter-base circuit ensures that current is switched from one collector to the other cleanly and rapidly, even at quite high working frequencies.

(4.6) A Practical Design

A practical oscillator based on the above principles, designed for energizing a measuring bridge at about 100 kc/s, is shown in Fig. 7, and the following results were obtained with it:

Power input = 120 mW.
Power output = 95 mW.
Efficiency = 79%.

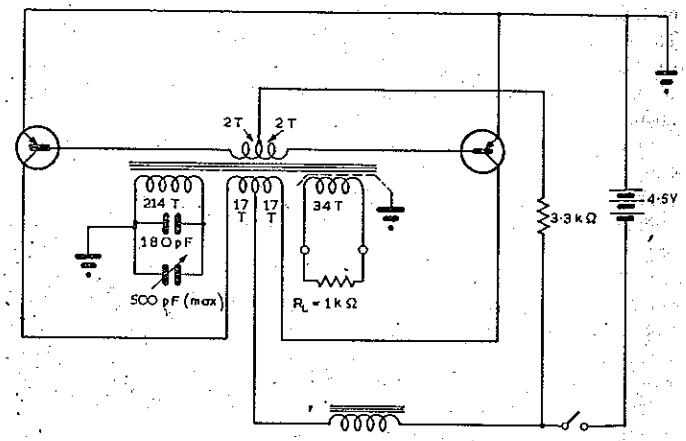

Fig. 7.—Practical circuit for current-switching oscillator.
Ordinary high-frequency alloy transistors are used. The main tuning inductor is wound on a ferrite pot core. The h.t. choke has a value of 0·8 mH.

The total power loss is thus 25 mW, and an approximate estimate of its distribution is

Tuned circuit : 11 mW.
Choke : 1 mW.
R_b : 8 mW.
Transistors : 5 mW.

In this particular model the transistors are called upon to

* In practice it is best to avoid values of L_2 greatly exceeding those here suggested, since squegging may occur.

develop much less output power than they are capable of providing in this type of circuit. The circuit described in Section 5.4 is a better illustration of the potentialities, with regard to power output, of circuits in which bottoming occurs throughout the whole of a 180° angle of flow.

(5) HIGH-EFFICIENCY VOLTAGE-SWITCHING OSCILLATOR

(5.1) Principle of Operation

The basic circuit of the voltage-switching oscillator is shown in Fig. 8. The bias arrangements necessary to ensure self-

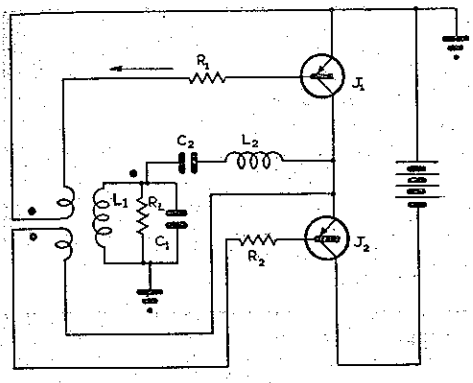

Fig. 8.—Basic circuit for voltage-switching oscillator.

starting are, however, omitted for clarity and will be described later.

The transistors act as switches, and the waveform of the voltage on the common lead between the two transistors is approximately a square wave [see Fig. 9(*a*)]. Since the series-tuned circuit L_2C_2 has ideally zero impedance at the fundamental frequency of this square wave, the fundamental component appears unattenuated across the parallel tuned circuit L_1C_1 to which the load R_L is connected. Thus the peak voltage appearing across R_L is ideally $4/\pi$ times the amplitude of the square wave, and the latter is half the h.t. supply voltage if the transistors are assumed to be ideal switches. This leads to the convenient design formula

$$\text{R.M.S. voltage across } R_L = \frac{\sqrt{2}}{\pi} \times V_{ht} = 0{\cdot}451 V_{ht} \quad . \quad . \quad (15)$$

However, the series-tuned circuit has a high impedance at the harmonic frequencies, so that only a small current at third- and other odd-harmonic frequencies flows to the tuned circuit L_1C_1, i.e. the current in L_2C_2 is approximately sinusoidal [see Fig. 9(*f*)]. This current is supplied in turn by the two transistors, so that the collector current of each transistor alternates between approximately a half sine wave and zero during successive half-cycles, as shown in (*e*).

The resistors in the base circuits are made low enough in value to ensure that, when collector current is flowing, the base current is always adequate to keep the transistors bottomed, and since the base-current waveform, shown in (*c*), also consists approximately of half sine waves, it keeps in step with the demand for collector current.

The mechanism whereby conduction is transferred from one transistor to the other will now be examined in greater detail.

Suppose that the end of the conduction time of transistor J_1 is approaching. Its base current, whose normal direction is shown by the arrow in Fig. 8, reaches zero, but, owing to hole-storage effects, it goes through zero and flows for a short time in the opposite direction to the arrow, as may be seen in Fig. 9(*c*). When the minority-carrier concentration has been cleared, the base current falls fairly rapidly back to zero, and the transistor is then 'off' as far as passing collector current in the normal direction is concerned. Just what occurs as a result of J_1 being thus turned off depends on the instantaneous current in L_2 at that time, and this, in turn, depends on three factors:

(*a*) The effective time delay in turning off, due to hole storage.
(*b*) Whether L_2C_2 is tuned to precisely the same frequency as L_1C_1.
(*c*) The effective bias voltage in the base circuit (in a practical circuit such as Fig. 10).

Suppose these factors are such that an appreciable current in L_2 is still flowing from right to left at the instant J_1 becomes non-conductive. Since the current in L_2 cannot suddenly cease, and since it can no longer be supplied by J_1, it must be supplied by inverted conduction of J_2 (i.e. the emitter acts as a collector and vice versa). To secure this, a large negative-going voltage step occurs on the collector of J_1. This inverted conduction of J_2 continues for a short time until the current in L_2 has reached zero. If, by that time, the base-drive voltage has brought J_2 into a state in which it is capable of adequate conduction in the normal direction, then, when the current in L_2 starts to flow from left to right, it flows down through J_2, the transistor remaining bottomed for the rest of the conduction period.

When Figs. 9(*a*) to (*f*) were obtained, the circuit was so adjusted that the current in L_2 reached zero at almost the same instant that one transistor was turned off, so that inverted conduction of the other transistor was not necessary.

By slightly lowering the resonant frequency of the series-tuned circuit with respect to that of the parallel-tuned circuit, Figs. 9(*g*) and (*h*) were obtained; each spike on waveform (*g*) indicated the presence for a short time of a collector-emitter voltage of reversed polarity across the corresponding transistor. Careful inspection of waveform (*h*) shows that collector current is turned off before it would otherwise have reached zero, and that, for a short time at the beginning of the collector-current pulse, the collector current flows in the reverse direction.

On experimenting with the circuit values, it is found that various conditions may be obtained, giving different detailed effects during the switchover time, but, provided that these effects are not exaggerated, they do not exert any great influence on the overall performance of the circuit.

A condition which should be avoided, however, is that in which one or both transistors fail to remain bottomed during some part of their conduction time. This failure shows up as a dip in the top or bottom of the voltage square wave on the lead joining the transistors. If this effect occurs anywhere near the middle of the conduction time, it results in greatly increased transistor dissipation, and the base resistors should be lowered in value to provide the increased base current necessary to maintain bottoming. In choosing the initial values for these resistors, due allowance should be made for the considerably reduced value of α' that is exhibited when a transistor is operated at high peak collector currents.

(5.2) Arrangements to ensure Self-Starting

In order to ensure that oscillation will begin to build up when the h.t. supply is switched on, it is necessary to arrange that both transistors are initially biased into the conducting state. A system which achieves this result with very little extra power dissipation is shown in the practical circuit of Fig. 10, and involves the use of two diodes. Before oscillation has built up, currents in R_3 and R_4 flow to the bases of the two transistors and the diodes are reverse-biased. There is d.c. negative feedback, since a change in the voltage on the lead between the

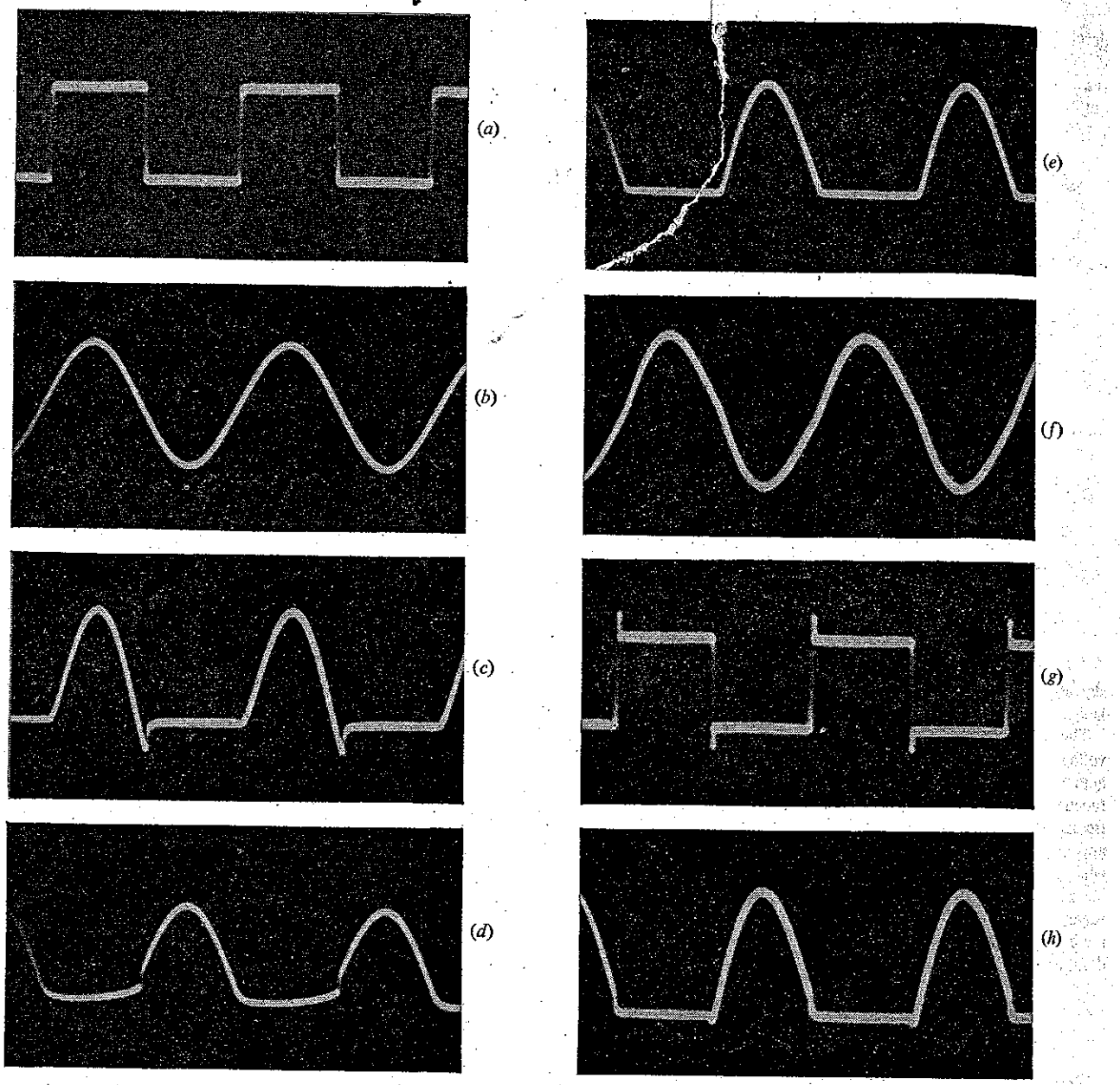

Fig. 9.—Waveforms for voltage-switching oscillator (Fig. 10 circuit).

(*a*) Voltage at common lead between transistors.
(*b*) Voltage across load.
(*c*) Base current of transistor J_1.
(*d*) Base voltage of transistor J_1.
(*e*) Collector current of transistor J_2.
(*f*) Current in series inductor.
(*g*) and (*h*) As (*a*) and (*e*) but with effective tuning capacitance of series-tuned circuit increased slightly.

transistors will increase one base current and decrease the other, and an equilibrium state for starting in which neither transistor is bottomed is therefore ensured.

When oscillation has built up, however, the mean base currents greatly exceed the currents in R_3 and R_4, and most of the current flows in the diodes. The capacitors connected across the diodes keep the diode voltages approximately constant once oscillation has built up, and permit the flow of reverse base current during the switching-off process.

It is possible to replace the diodes by resistors, but R_3 and R_4 must then be of much lower value and the power loss is considerably greater.

(5.3) Choice of Tuned-Circuit Values

Referring to the basic circuit of Fig. 8, the tuned circuit L_1C_1 has a loaded Q-factor of approximately $R_L/\omega_0 L_1$. At the resonant frequency, $\omega_0/2\pi$, of the tuned circuits, the series resistance of the series-tuned circuit is effectively R_L, and so, in this limited sense, the series-tuned circuit may be said to have a loaded Q-factor of $\omega_0 L_2/R_L$. If these Q-factors are made equal, it may be shown that the peak magnetic energy will be the same in the two inductors, and if the inductors themselves have the same unloaded Q-factors, assumed much higher than the loaded values, the same power dissipation will occur in each. These conditions are considered to be the most suitable choice for

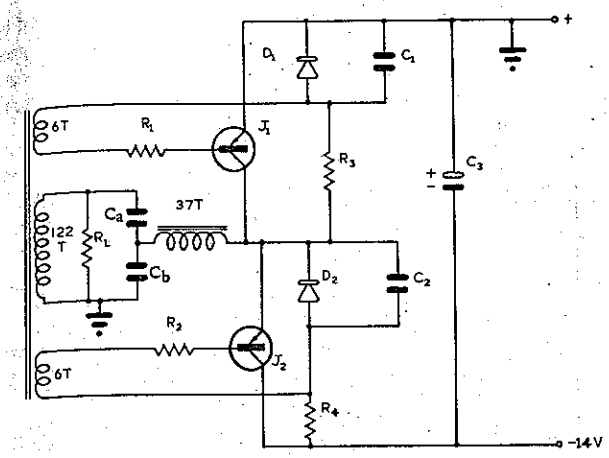

Fig. 10.—Practical circuit for voltage-switching oscillator.

R_1, R_2. 100 ohms.
R_3, R_4. 100 kilohms.
R_L. 3 kilohms.
C_a. 3900 pF.
C_b. 0·0352 μF.
C_1, C_2. 0·1 μF.
C_3. 25 μF.

Both inductors are wound on Ferroxcube type LA2 pot cores. The transistors are type OC44.
D_1 and D_2 are germanium junction diodes.

practical designs, the two inductors being of the same physical size.

Normally, a suitable loaded Q-factor to adopt for both tuned circuits is 3, which keeps the tuned-circuit losses very low. But since there are two tuned circuits contributing to reduction of harmonic distortion, these low losses are not accompanied by undesirably high distortion.

The third-harmonic distortion in the output voltage, assuming equal loaded Q-factors for the two tuned circuits, is given approximately by

$$\frac{3}{64Q^2} \times 100\% \quad . \quad . \quad . \quad . \quad . \quad . \quad (16)$$

Thus, with the recommended Q-factor of 3, the third-harmonic distortion is approximately 0·5%, and higher-order odd harmonics have a magnitude approximately inversely proportional to the cube of their order, and are normally negligible.

(5.4) Practical Design

The experimental 45 kc/s oscillator shown in Fig. 10 uses two small high-frequency transistors, each having a maximum permitted collector dissipation of 70 mW. The oscillator has been in continuous operation for over 3 500 hours at an output power of about 1·4 watts, the overall efficiency being approximately 85%. No change in any waveform has been observed over this period. The total power dissipation in the transistors is less than 50 mW.

Other figures obtained from measurements on this oscillator are as follows:

Peak collector current	350 mA (approximately)*
Third-harmonic distortion	0·42%
Second-harmonic distortion	0·1% (approximately)
Feed current on no-load	17 mA (equivalent to 240 mW)

It will be seen that the arrangement of the tuned circuits in Fig. 10 is not the same as in the basic circuit of Fig. 8. On calculating values for the basic circuit it was found that L_1 was inconveniently small and C_1 inconveniently large. The obvious solution would have been to replace L_1C_1 by a circuit of more practical L/C ratio and connect the L_2C_2 circuit to a tapping on the coil. It is possible to avoid the necessity for such a tapping, however, by exploiting the equivalence of the two circuits shown in Fig. 3. If the right ratio for $(C_a + C_b)/C_a$ is chosen, it is practicable to use $(C_a + C_b)$ as the tuning capacitance for the series-tuned circuit, thus saving a capacitor. This technique has been adopted in the circuit of Fig. 10.

If the loaded Q-factors for the series- and parallel-tuned circuits are made equal, as recommended in Section 5.3, the ratio $C_b : C_a$ which allows $(C_a + C_b)$ to be the only tuning capacitance for the series-tuned circuit may be shown to be

$$\frac{C_b}{C_a} = Q^2 \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (17)$$

Thus if $Q = 3$, as adopted in the circuit of Fig. 10, then C_b equals $9C_a$ and the effective transformer ratio, $(C_a + C_b)/C_a$, is 10. In this case, the load resistance to be connected across the parallel-tuned circuit is 100 times the resistance presented to the transistors at fundamental frequency.

(5.5) Conclusions

Considering the oscillators described in Section 4 and this Section, the former would seem better suited to widespread application since it uses considerably fewer components and is capable of operating satisfactorily at higher frequencies. However, the present oscillator has the following advantages, which make it more suitable for certain applications:

(*a*) The maximum voltage appearing across each transistor is approximately equal to the h.t. voltage, whereas in the oscillator of Section 4 it is πV_{ht}. Consequently the present oscillator can operate from π times the h.t. supply voltage of the previous design, and, for a given power output, will require only about $1/\pi$ times the h.t. current. The peak transistor current in the present oscillator is, however, π times the mean current, and so will be about the same, for the same power output, as in the previous oscillator, since, in the latter, it is equal to the mean current. Thus the peak current in the transistors when conducting is about the same in each oscillator, but since it is maintained for the whole 180° conduction angle in the previous oscillator, a greater mean power dissipation in the transistors would be expected in the previous oscillator, for a given output power. The present oscillator is thus capable of higher collector efficiency.

(*b*) For the same power output and efficiency, the present oscillator gives considerably less harmonic distortion at full load. If the load resistance is raised, the distortion remains approximately constant, whereas, in the previous oscillator, the distortion falls as the load resistance is raised.

(*c*) The present oscillator does not suffer damage if the output is short-circuited, whereas in the previous one the transistors would immediately be ruined.

(6) 'LONG-TAILED-PAIR' OSCILLATOR

(6.1) The Basic Circuit

In many low-power oscillator applications, high efficiency is not in itself of great importance, whereas simplicity of design calculations, and a performance which is readily predictable and relatively independent of variations in transistor parameters, represent highly desirable characteristics. A simple circuit which has been found very useful for such applications is shown in Fig. 11(*a*).

In this circuit, the current flowing in R_e is switched alternately through J_1 and J_2 by the feedback voltage applied between the bases. This voltage is quite uncritical and 1 volt (peak) is sufficient to give satisfactorily quick switching action. When J_1 is conducting, the collector current is given, to a close approximation, by V_1/R_e, and so the tuned circuit is fed with a current square wave of peak-to-peak magnitude V_1/R_e and a mark/space

* This current is, of course, far above the maker's rating, but the limited experience gained so far suggests that transistors can withstand this treatment so long as the mean collector dissipation does not exceed the maker's rating.

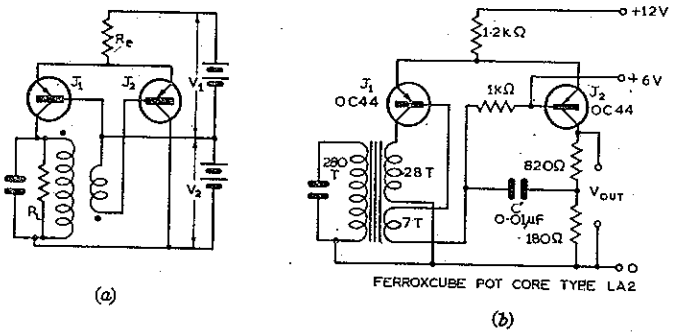

Fig. 11.—Long-tailed-pair oscillator circuits.
(*a*) Basic circuit giving sine-wave output.
(*b*) Modified circuit giving square-wave output.

ratio of unity. The peak value of the fundamental component of this square wave is $2V_1/\pi R_e$, and the peak value, V_{max}, of the approximately sine-wave voltage at the collector is therefore given by

$$V_{max} = \frac{2V_1 R_L}{\pi R_e} \quad . \quad . \quad . \quad . \quad . \quad (18)$$

where R_L includes the tuned-circuit losses. It is necessary to make V_{max} considerably less than V_2, in order to avoid any risk of J_2 bottoming.

Performance in reasonable agreement with eqn. (18), say within $\pm 20\%$, is obtained up to a frequency in the region of a quarter of the α cut-off frequency of the transistors.

(6.2) Harmonic Distortion

The oscillator is similar to that described in Section 4 in that the tuned circuit is fed with a current of square waveform, and the third-harmonic distortion is therefore approximately as given by eqn. (12). Thus with a Q-factor of 125, which can often be easily obtained in practice, the third-harmonic distortion is 0·1%. All the other harmonics are much lower still.

(6.3) Provision of Square-Wave Output

The circuit may also be used to provide a square wave of current or voltage, controlled accurately in frequency by a high Q-factor tuned circuit. This fact has been exploited very beneficially in one of the primary oscillators of an all-transistor beat-frequency oscillator.*

A voltage square-wave output may be obtained by inserting a resistor in the collector lead of J_2. With the circuit otherwise as in Fig. 11(*a*), the square wave would have a rounded top, owing to the current variation that results from the variation in base voltage while J_2 is conducting; the higher V_1 and R_e are made, the less is the extent of this rounding. The effect may be eliminated, however, if the base of J_2 instead of that of J_1 is taken to the junction of the two supply batteries. With this modification, it is the waveform of the current fed to the tuned circuit that is a distorted square wave. It may then be necessary to reduce the dynamic resistance of the tuned circuit to prevent the voltage across J_1 reaching zero on peak positive excursions of the collector voltage, which coincide with peak negative excursions of the emitter voltage.

(6.4) Modification to give Trigger Action

A much improved square-wave output may be obtained if the circuit is made to function in the same manner as a multivibrator during the change-over action only. This may be achieved by the modification shown in Fig. 11(*b*). This circuit was designed for a recent application and generates a 12 kc/s square wave with rise and fall times of a fraction of a microsecond, some actual waveforms being shown in Fig. 12.

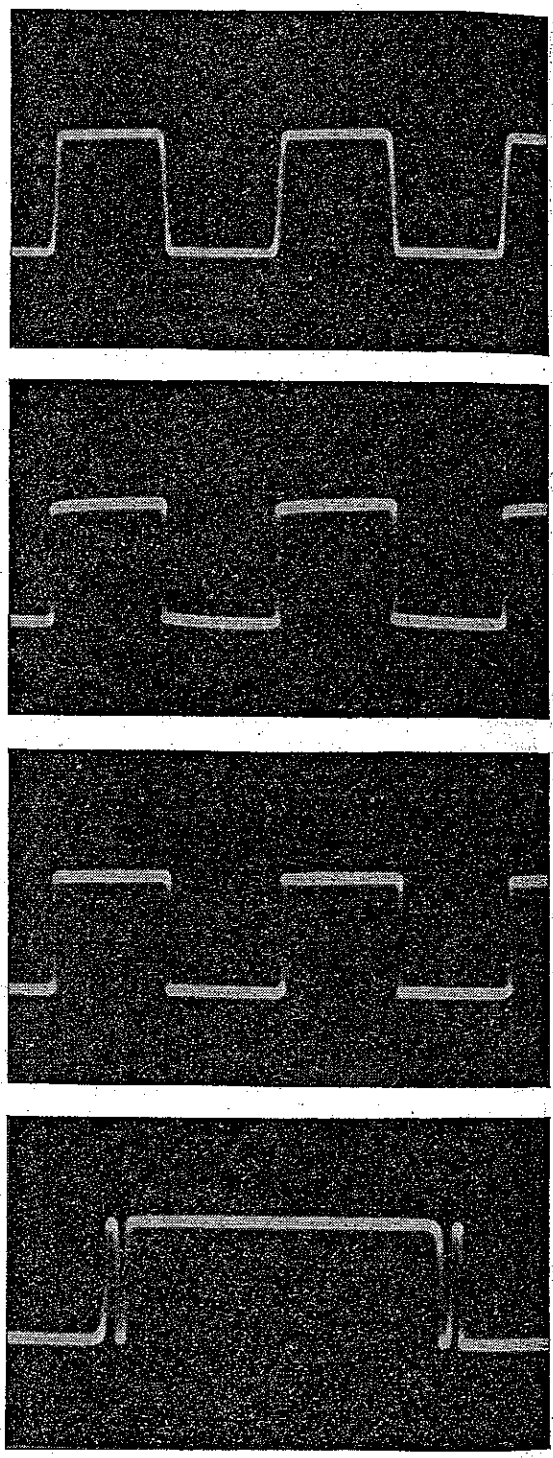

Fig. 12.—Output-voltage waveforms for circuit of Fig. 11(*b*).
(*a*) C′ disconnected and 1-kilohm resistor in base circuit short-circuited.
(*b*) Circuit exactly as shown.
(*c*) As for (*b*) but with C′ increased to 1μF.
(*d*) As for (*b*) but with C′ reduced to 500 pF.

* In this beat-frequency oscillator, a sine-wave current from one 'long-tailed-pair' oscillator is fed to a balanced transistor switching circuit. The 'switch' is operated by a square-wave current from another 'long-tailed-pair' oscillator, thus generating the wanted beat frequency. The total harmonic distortion is less than 0·1%.

Comparing Figs. 12(*b*) and (*c*), it is seen that the best waveform is obtained when C' is very large. In this case, however, an inconvenient feature is that, on switching on the h.t. supply, the circuit oscillates simply as an emitter-coupled multivibrator, at some quite low frequency, instead of in the wanted mode. By momentarily connecting the emitter of J_2 to the h.t. negative supply, the circuit may be got into the wanted mode; this was done to obtain the waveform of Fig. 12(*c*). When operating in the wrong mode, the tuned-circuit waveform consists merely of a succession of small-amplitude exponentially-decaying transient oscillations.

For completely reliable self-starting in the correct mode, the oscillation frequency of the circuit considered as a multivibrator should be higher than the tuned-circuit frequency. On switching on, the circuit then starts up as a multivibrator, going periodically through a state in which both transistors are conducting, and therefore in which there is positive feedback suitable for building up the sine-wave oscillation. Once the latter has reached sufficient amplitude, it takes charge of the frequency and the free-running multivibrator action ceases. If C' is reduced too far, however, effects such as that shown in waveform (*d*) are produced, but in practice, there is a wide range of values for C' throughout which the desired behaviour is obtained.

(7) ACKNOWLEDGMENTS

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(9) APPENDICES

(9.1) Magnitude of Current Fluctuation in L_2 of Fig. 5

Fig. 13(*a*) represents the voltage across L_2 in Fig. 5. Between $t = 0$ and $t = t_1$ the waveform may be represented by

$$v = -V_{max} \sin \omega t + \frac{2}{\pi} V_{max} \quad . \quad . \quad . \quad . \quad (19)$$

The current waveform over this time interval is given by

$$i = \frac{1}{L_2} \int v dt$$

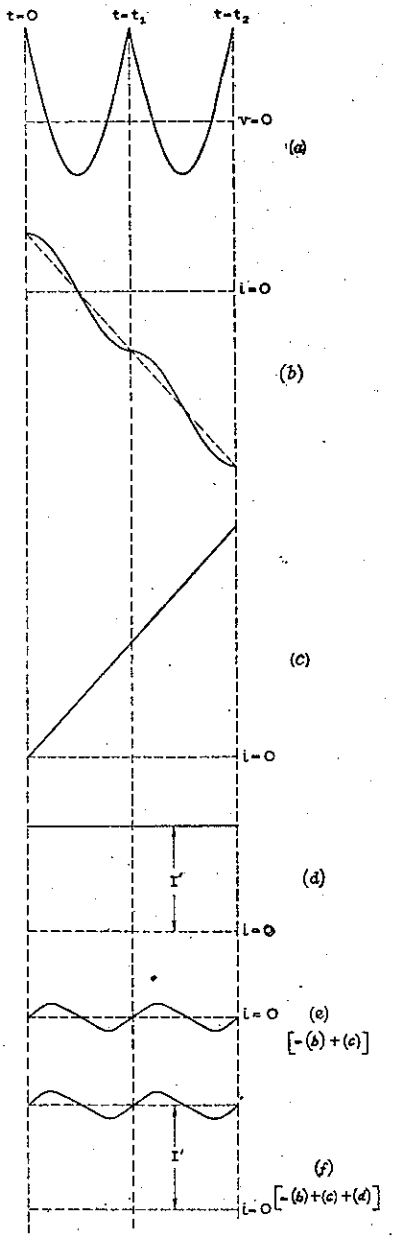

Fig. 13.—Waveforms relating to Section 9.

which leads to

$$i = \frac{V_{max}}{L_2}\left(\frac{1}{\omega} \cos \omega t + \frac{2}{\pi} t\right) + I' \quad . \quad . \quad . \quad (20)$$

in which I' is the constant of integration.

The three current components represented by this equation are shown in Figs. 13(*b*), (*c*) and (*d*). The waveforms may be extended beyond $t = t_1$, since their shapes must be the same during each successive time interval 0–t_1, t_1–t_2, etc., and also there can be no sudden change of current at these instants. The total waveform of the current in L_2 is then obtained by adding together the component waveforms. Figs. 13(*b*) and (*c*) must necessarily have numerically the same mean slopes, so that their sum has zero mean slope (otherwise the current would tend towards infinity). The addition may conveniently be done by first drawing in the dotted line on Fig. 13(*b*) and measuring the intercepts between this line and the waveform,

thus obtaining the ordinates for drawing Fig. 13(*e*). The total current in L_2 is then obtained by adding on the d.c. component given by (*d*), resulting in (*f*). (The d.c. component may be determined from a knowledge of the h.t. voltage, power output and efficiency.)

Since Fig. 13(*f*) is the integral of (*a*), its maxima and minima must occur when (*a*) passes through zero, i.e. when $\sin \omega t = 2/\pi$. This gives two values of t during the time interval 0–t_1, and by substituting these in eqn. (20) and subtracting the values of i obtained, the peak-to-peak value of the current waveform may be derived. This is given by

$$I_{pp} = 0{\cdot}421\frac{V_{max}}{\omega L_2} \quad . \quad . \quad . \quad . \quad . \quad (21)$$

If I_{pp} is made a quarter of the mean h.t. current, which is a reasonable practical choice, eqn. (21) gives

$$\tfrac{1}{4}I_{ht} = 0{\cdot}421\frac{V_{max}}{\omega L_2} \quad . \quad . \quad . \quad . \quad . \quad (22)$$

If the oscillator is assumed to be 100% efficient,

$$V_{ht}I_{ht} = \frac{1}{2}\frac{(2V_{max})^2}{R_L} \quad . \quad . \quad . \quad . \quad . \quad (23)$$

and from eqn. (9)

$$V_{ht} = \frac{2}{\pi}V_{max}$$

and so eqn. (23) becomes

$$\frac{I_{ht}}{V_{max}} = \frac{\pi}{R_L} \quad . \quad . \quad . \quad . \quad . \quad . \quad (24)$$

Eliminating I_{ht}/V_{max} between eqns. (22) and (24)

$$\omega L_2 = R_L \times \frac{4 \times 0{\cdot}421}{\pi}$$

$$= 0{\cdot}536R_L \quad . \quad . \quad . \quad . \quad . \quad . \quad (25)$$

(9.2) Magnetic Energy Stored in L_1 and L_2

Ignoring the alternating component of the current in L_2, the energy stored in L_2 is given by

$$W_{L2} = \tfrac{1}{2}L_2I_{ht}^2 \quad . \quad . \quad . \quad . \quad . \quad . \quad (26)$$

With L_2 chosen to make $I_{pp} = \frac{1}{4}I_{ht}$, and using eqn. (22), this stored energy may be expressed as

$$W_{L2} = 1{\cdot}42\frac{V_{max}^2}{\omega^2 L_2} \quad . \quad . \quad . \quad . \quad . \quad (27)$$

The peak current in L_1 is $2V_{max}/\omega L_1$, and so the peak energy stored in L_1 is given by

$$W_{L1\,max} = \tfrac{1}{2}L_1 \times \frac{4V_{max}^2}{(\omega L_1)^2}$$

$$= \frac{2V_{max}^2}{\omega^2 L_1} \quad . \quad . \quad . \quad . \quad . \quad . \quad (28)$$

If the loaded Q-factor is 10, then $\omega L_1 = R_L/10$, and it follows from this relationship and eqn. (25) that

$$\frac{L_1}{L_2} = \frac{1}{10 \times 0{\cdot}536} = 0{\cdot}187 \quad . \quad . \quad . \quad . \quad (29)$$

Finally, from eqns. (27), (28) and (29) may be obtained

$$\frac{W_{L2}}{W_{L1\,max}} = \frac{1{\cdot}42}{2} \times 0{\cdot}187 = 0{\cdot}013\,2 \quad . \quad . \quad (30)$$

In other words, when $I_{pp} = \frac{1}{4}I_{ht}$, and the loaded Q-factor is 10, the magnetic energy stored in L_2 is approximately 13% of the peak magnetic energy stored in L_1.